5673053

B.Tech. DEGREE EXAMINATION JANUARY 2023

Third Semester

Information Technology

COMPUTER ORGANIZATION

(2013-14 Regulations)

Time: Three Hours **Maximum:75 marks**

PART-A---(10*2-20 Marks)

Answer ALL questions

1. **State the uses of Computer.**

It refers to the operational units and their interconnections that realize the architectural specifications. It describes the function of and design of the various units of digital computer that store and process information.

2. **List the input and output devices.**

Input devices

- Joysticks
- Trackballs
- Mouse
- Microphones

Output devices

- Printers
- Monitor
- Speakers
- Projectors.

3. **What is meant by execution?**

- To begin executing a program, the address of first instruction must be placed in PC.
- The processor control circuits use the information in the PC to fetch & execute instructions one at a time in the order of increasing order.
- This is called Straight line sequencing.During the execution of each instruction,the PC is incremented by 4 to point the address of next instruction.

4. **Specify the importance of Nano programming.**

- In most micro programmed processors, an instruction fetched from memory is interpreted by a microprogram stored in a single control memory.
- However,in few microprogrammed processors,the microinstruction do not directly used by the decoder to generate control signals.
- Instead they are used to accesses cond control memory called a Nano control memory(nCM).

5. Mention the concept of pipelining.

Pipelining

- It is a particularly effective way of organizing concurrent activity in a computer system.

Types of Pipeline

- Instructional pipeline
- Arithmetic pipeline

Instructional pipeline-where different stages of an instruction fetch and execution are handled in a pipeline.
Arithmetic pipeline-where different stages of an arithmetic operation are handled a long the stages of a pipeline.

6. Write the use of instruction.

instructions are much better suited to pipeline execution than others. Two key aspects ofmachine instructions are;

- Addressing modes and Conditional code flags
- One drawback of micro programmed control is the slower operation because of the time it takesto fetch instruction s from the control store.
- Faster operation is achieved if the next instruction is pre fetched while three current one is beingexecuted

7. Compare RAM with ROM.

RAM	ROM
The memory devices used for primary memory are semiconductor memories.	The secondary memory devices are magnetic and optical memories.
The primary memory is volatile.	The secondary is non-volatile
The primary memory is composed of programs and data that are presently being used by the micro-processor	The secondary memory is enough capable to store huge amount of information.
Primary memory is known as main memory	Auxiliary memory is known as additional memory or back memory

8. Give the principle of cache memory.

- It is a small, fast memory that is inserted between the larger slower main memory and the processor.
- It holds the currently active segments of a program and their data.

9. Indicate the concept behind interrupts.

- When a program enters a wait loop, it will repeatedly check the device status.
- During this period, the processor will not perform any function.
- The interrupt request line will send a hardware signal called the interrupt signal to the processor.

On receiving this signal, the processor will perform the useful function during the waiting period.

10. **Specify the need of USB.**

- USB has a serial bus format which satisfies the low-cost and flexibility requirements.
- Clock and data information are encoded together and transmitted as a single signal.
- There are no limitations on clock frequency or distance arising from data skew, and
- hence it ispossible to provide a high data transfer bandwidth by using a high clock
- frequency.
- To accommodate a large number of devices that can be added / removed at any time, the USB hasthe tree structure.

PART-B-(5*11=55 Marks)
Answer ALL the questions

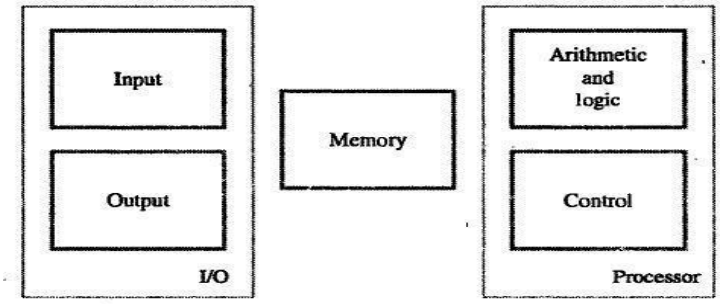
UNIT-I

11. Outline the function of computers with suitable diagram.

A computer consists of 5 main parts.

- Input Memory
- Arithmetic and logic
- Output
- Control Units

Functional units of a Computer



- Input unit accepts coded information from human operators, from electromechanical devices such as keyboards, or from other computers over digital communication lines.
- The information received is either stored in the computers memory for later reference or immediately used by the arithmetic and logic circuitry to perform the desired operations.
- The processing steps are determined by a program stored in the memory. Finally the results are sent back to the outside world through the output unit. All of these actions are coordinated by the control unit.

Input Unit:

- Computers accept coded information through input units, which read the data.
- Whenever a key is pressed, the corresponding letter or digit is automatically translated into its corresponding binary code and transmitted over a cable to either the memory or the processor.Some input devices are
- Joysticks
- Trackballs
- Mouses
- Microphones (Capture audio input and it is sampled & it is converted into digital codes for storage and processing)

Memory Unit:

It stores the programs and data. There are 2 types of storage classes

- Primary

- Secondary Primary Storage: It is a fast memory that operates at electronic speeds. Programs must be stored in the memory while they are being executed.

RAM:

Memory in which any location can be reached in short and fixed amount of time after specifying its address is called RAM. Time required to access 1 word is called Memory Access Time.

Cache Memory: The small,fast,RAM units are called Cache. They are tightly coupled with processor to achieve high performance.

Main Memory: The largest and the slowest unit is called the main memory.

ALU:

- Most computer operations are executed in ALU. Consider a example,Suppose 2 numbers located in memory are to be added.
- They are brought into the processor and the actual addition is carried out by the ALU. The sum may then be stored in the memory or retained in the processor for immediate use.
- Access time to registers is faster than access time to the fastest cache unit in memory.

Output Unit:

Its function is to send the processed results to the outside world. eg.Printer Printers are capable of printing 10000 lines per minute but its speed is comparatively slower than the processor.

Control Unit:

- The operations of Input unit, output unit, ALU are co-ordinate by the control unit. The control unit is the Nerve centre that sends control signals to other units and senses their states.
- Data transfers between the processor and the memory are also controlled by the control unit through timing signals.
- The operation of computers are the computer accepts information in the form of programs and data through an input unit and stores it in the memory.

(OR)

12. Compare the fixed point operations with floating point operations with example.

- In computing, a fixed-point number representation is a real data type for a number that has a fixed number of digits after (and sometimes also before) the radix point (e.g., after the decimal point '.' in English decimal notation).
- Fixed-point number representation can be compared to the more complicated (and more computationally demanding) floating point number representation.
- Fixed-point numbers are useful for representing fractional values, usually in base 2 or base 10, when the executing processor has no floating point unit (FPU) or if fixed-point provides improved performance or accuracy for the application at hand. Most low-cost embedded microprocessors and microcontrollers do not have an FPU.

Representation

- A value of a fixed-point data type is essentially an integer that is scaled by a specific factor determined by the type.
- For example, the value 1.23 can be represented as 1230 in a fixed-point data type with scaling factor of 1/1000, and the value 1230000 can be represented as 1230 with a scaling factor of 1000.
- Unlike floating-point data types, the scaling factor is the same for all values of the same type, and does not change during the entire computation.
- The scaling factor is usually a power of 10 (for human convenience) or a power of 2 (for computational efficiency). However, other scaling factors may be used occasionally,
- **E.g.** a time value in hours may be represented as a fixed-point type with a scale factor of 1/3600 to obtain values with one-second accuracy.
- For example, consider a fixed-point type represented as a binary integer with b bits in two's complement format, with a scaling factor of 1/2f (that is, the last f bits are fraction bits): the minimum representable value is −2b-1/2f and the maximum value is (2b-1-1)/2f.

Operations

- To convert a number from a fixed point type with scaling factor R to another type with scaling factor S, the underlying integer must be multiplied by R and divided by S; that is, multiplied by the ratio R/S.
- Thus, for example, to convert the value 1.23 = 123/100 from a type with scaling factor R=1/100 to one with scaling factor S=1/1000, the underlying integer 123 must be multiplied by (1/100)/(1/1000) = 10, yielding the representation 1230/1000. If S does not divide R (in particular, if the new scaling factor R is less than the original S), the new integer will have to be rounded.
- The rounding rules and methods are usually part of the language's specification. To add or subtract two values the same fixed-point type, it is sufficient to add or subtract the underlying integers, and keep their common scaling factor.
- The result can be exactly represented in the same type, as long as no overflow occurs (i.e. provided that the sum of the two integers fits in the underlying integer type.) If the numbers have different fixedpoint types, with different scaling factors, then one of them must be converted to the other before the sum.

Floating point Representation:

To represent the fractional binary numbers, it is necessary to consider binary point.If binary point is assumed to the right of the sign bit ,we can represent the fractional binary numbers as given below,

$$B=(b0 *20+b-1*2-1+b-2* 2-2+….+ b-(n-1)*2-(n-1)$$

With this fractional number system,we can represent the fractional numbers in the following range,

$$-1 < F < 1 – 2 -(n-1)$$

- The binary point is said to be float and the numbers are called floating point numbers.
- The position of binary point in floating point numbers is variable and hence numbers must be represented in the specific manner is referred to as floating point representation.
- The floating point representation has three fields.They are,

- Sign
- Significant digits and
- Exponent.

B= (b0 * 20 +b-1 * 2-1 + b-2 * 2-2 +….+ b-(n-1) * 2-(n-1))

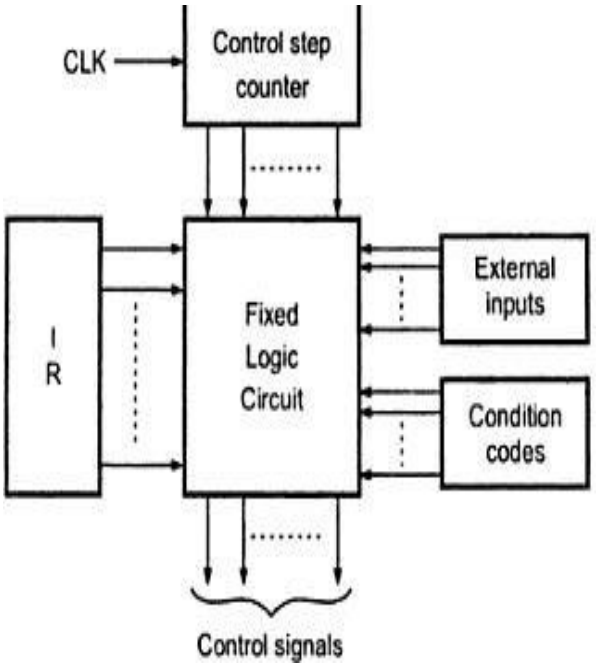
Eg: 111101.1000110□1.111101100110 *25

Where , 25 <-Exponent and scaling factor.

UNIT-II

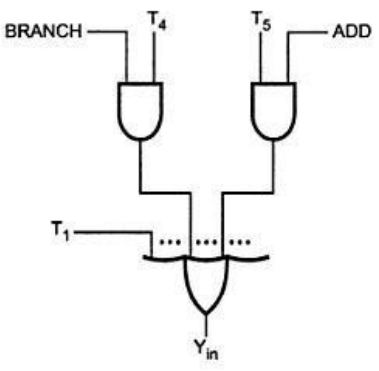
13. Illustrate the function of Hardwired Control.

- The control units use fixed logic circuits to interpret instructions and generate control signals from them.
- The fixed logic circuit block includes combinational circuit that generates the required control outputs for decoding and encoding functions**.**

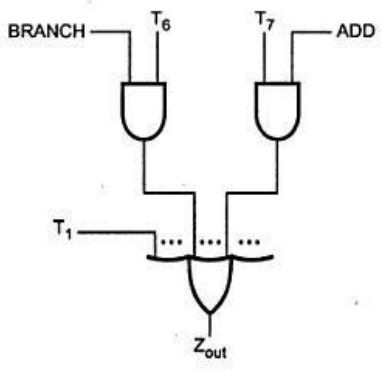


- Let us see how the encoder generates signal for single bus processor organization own in Yin. The encoder circuit implements the following logic function to generate Yin.

$$Y_{in} = T_1 + T_5 \cdot ADD + T_4 \cdot BRANCH + \ldots$$



Generation of the Y_{in} control signal



Generation of the Z_{out} control signal

Instruction decoder

- In the instruction decoder, the instruction loaded in the IR.
- If IR is an 8-Bit register then instruction decoder generates 28, i.e 256 lines; one for each instruction.
- According to code in the IR, only one line of decoder goes high i.e,set to 1 and all other lines are setto 0.

Step decoder

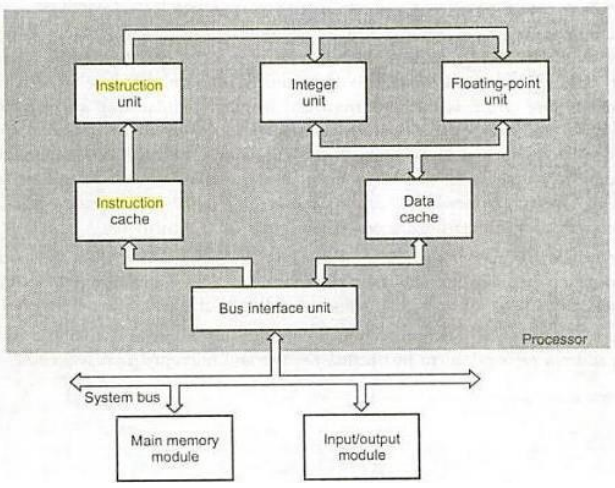
- The step decoder provides a separate signal line for each step or time slot, in a control sequence.

Encoder

- The decoder gets in the input from instruction decoder, step decoder, external inputs and conditioncodes.
- The encoder circuit implements the following logic function to generate
  YinYin = T1 + T5 . Add + T . BRANCH+…
- The Yin signal is asserted during time interval T1 for all instructions, during T5 for an ADD instruction, during T4 for an unconditional branch instruction, and so on.
- As another example, the logic function to generate Zout signal can given
  byZout = T2 + T7 . ADD + T6 . BRANCH +….

A Complete processor

- It consists of
  - * Instruction unit
  - * Integer unit
  - * Floating-point unit
  - * Instruction cache
  - * Data cache
  - * Bus interface unit
  - * Main memory module
  - * Input/ Output module



Block diagram of Complete Processor

(Or)

14. Outline the functions of Micro Programmed Control.

- Every instruction in a processor is implemented by a sequence of one or more sets of concurrent micro operations.
- Each micro operation is associated with a specific set of control lines which, when activated, causesthat micro operation to take place.
- Since the number of instructions and control lines is often in the hundreds, the complexity of hardwired control unit is very high.
- The microprogrammed control unit,
  * Control memory
  * Control address register
  * Micro instruction register
- Microprogram sequencer

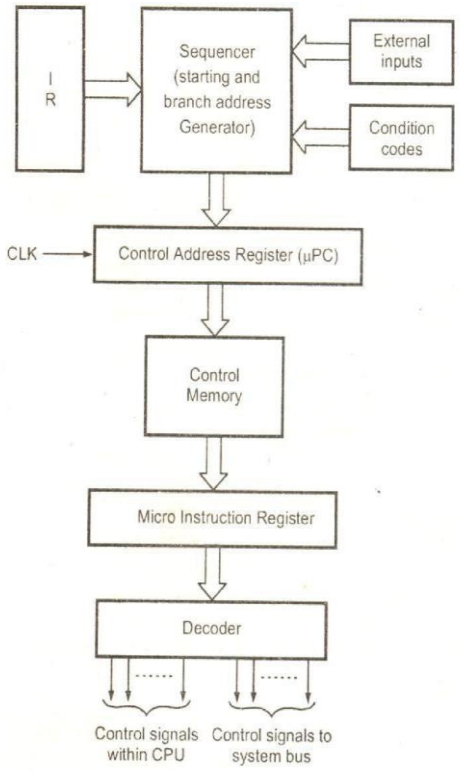
Advantages of Microprogrammed control

- It simplifies the design of control unit. Thus it is both, cheaper and less error phrone implement.
- Control functions are implemented in software rather than hardware.

Disadvantages of Microprogrammed control

- A microprogrammed control unit is somewhat slower than the hardwired control unit, because timeis required to access the microinstructions from Control Memory.
- The flexibility is achieved at some extra hardware cost due to the control memory and its access circuitry.

- Let us assume that the source operand can be specified in the following addressing modes:
  * Indexed
  * Auto increment
  * Auto decrement

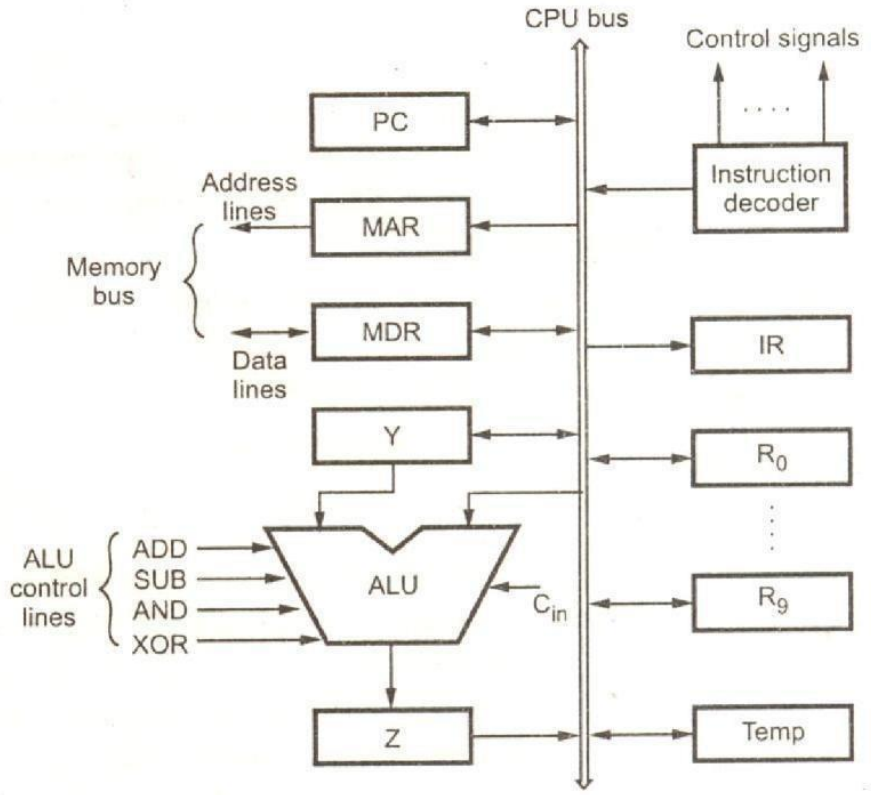


- Each box in the flowchart corresponds to a microinstruction that controls the transfers and operationsindicated within the box.
- The microinstruction is located at the address indicated by the number above the upper right-handcorner of the box.
- During the execution of the microinstruction, the branching takes place at point A.

Wide-Branch Addressing

- Generating branch addresses becomes more difficult as the number of branches increases.
- In such situations programmable logic array can be used to generate the required branch addresses.

The simple and inexpensive way of generating branch addresses is known as wide-branch addressing.



UNIT-III

15. Compare polling approach with interrupt approach.

- The dispatch unit dispatches the instructions in the order in which they appear in the program.
- But their execution may be completed in the different order.
- For example, execution of I2 is completed before the complete execution of I1. Thus the executionof the instructions is completed out of order.
- If there is a data dependency among the instructions, the execution of the instructions is delayed.
- For example, if the execution of I2 needs the results of execution of I1, I2 will be delayed.
- If such dependencies are handled correctly, the execution of the instructions will not be delayed.
- There are two causes of exceptions,
    * Bus error (during an operand fetch)
    * Illegal operation (e.g. Divide by zero)
- The two types of exceptions,
    * Imprecise exceptions
    * Precise exceptions

Imprecise exception

- Consider the pipeline timing, the result of operation of I2 is written into the register file in cycle 4.
- If instruction I1 causes an exception and succeeding instructions are permitted to complete execution, then the processor is said to have imprecise exceptions.
- Because of the exception by I1, program execution is in an inconsistent state.

Precise exception

- In the imprecise exception, consistent state is not guaranteed when an exception occurs.
- If the exception occurred then to guarantee a consistent state, the result of the execution of instructions must be written into the destination locations strictly in the program order.
- The result of execution of I2 is written to the destination in cycle 4 (W2). But the result of I1 iswritten to the destination in cycle 6 (W1). So step W2 is to be delayed until cycle 6.
- The integer execution unit has to retain the result of execution of I2. So it cannot accept instructionI4 until cycle 6.
- Thus in precise exception, if the exception occurs during an instruction, the succeeding instructions,may have been partially executed are discarded.
- If an external interrupt is received, the dispatch unit stops reading new instructions from the instruction queue.
- The instructions which are placed in the instruction queue are discarded.

The processor first completes the pending execution of the instructions to completion. The consistent state of the processor and all its registers is achieved.

(Or)

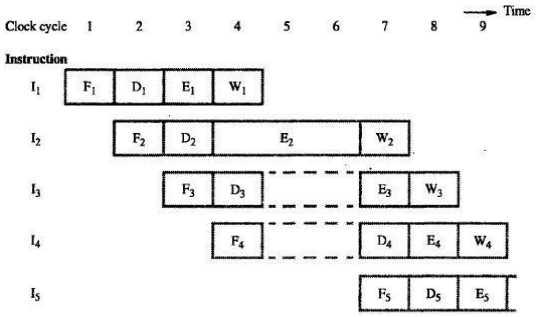
16. Summarize the various hazards in detail.

Hazard

- A pipeline hazard refers to a situation in which a correct program ceases to work correctly due toimplementing the processor with a pipeline.
- Any condition that causes the pipeline to stall is called a hazard

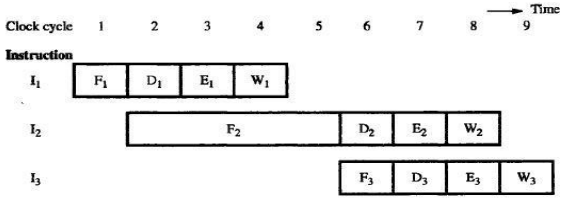
Data Hazard

- A data hazard is any condition in which either the source or the destination operands of an instruction are not available at the time expected in the pipeline.
- As a result, some operation has to be delayed, and the pipeline stalls.

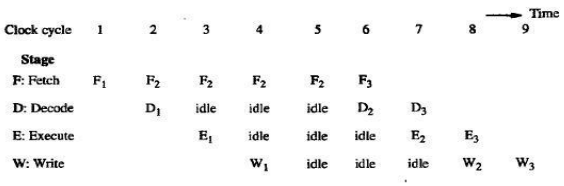


Control Hazards

- The pipeline may also be stalled because of a delay in the availability of an instruction.
- For example, this may a result of a miss in the cache, requiring the instruction to be fetched from themain memory.



(a) Instruction execution steps in successive clock cycles



(b) Function performed by each processor stage in successive clock cycles

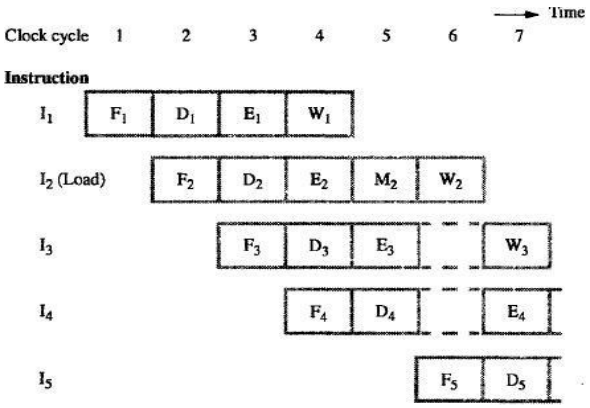
- Such hazards are often called control hazards or instruction hazards.

Structural Hazards

- A third type of hazard that may be encountered in pipelined operation is known as a

structuralhazard.

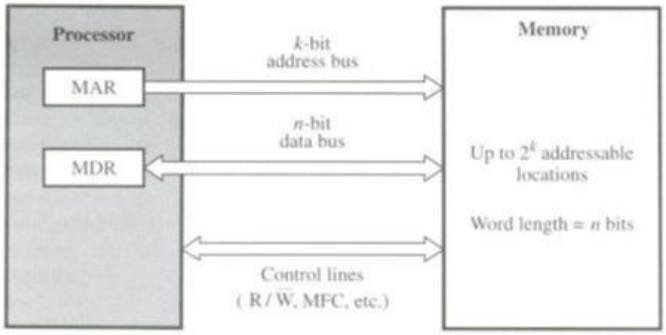
- This is the situation when two instructions requires the use of a given hardware resource at the sametime.
- The most common case in which this hazard may arise is in access to memory.
- Many processors use separate instruction and data caches to avoid this delay.
- Example of the structural hazard is shown below.
  Load X (R1),R2



UNIT-IV

17. Outline the types of Memories in detail.

- The maximum size of the memory that can be used in any computer is determined by the addressingscheme.
- If MAR is k bits long and MDR is n bits long, then the memory may contain upto 2K addressablelocations and the n-bits of data are transferred between the memory and processor.
- This transfer takes place over the processor bus.



Connection of Memory to Processor

RAM (Random Access Memory)

- In RAM, if any location that can be accessed for a Read/Write operation in fixed amount of time,it is independent of the location's address.

Cache Memory

- It is a small, fast memory that is inserted between the larger slower main memory and theprocessor.
- It holds the currently active segments of a program and their data.

Virtual memory

- The address generated by the processor does not directly specify the physical locations in thememory.
- The address generated by the processor is referred to as a virtual / logical address.
- The virtual address space is mapped onto the physical memory where data are actually stored.
- The mapping function is implemented by a special memory control circuit is often called thememory management unit.
- Only the active portion of the address space is mapped into locations in the physical memory.
- The remaining virtual addresses are mapped onto the bulk storage devices used, which are usuallymagnetic disk.
- As the active portion of the virtual address space changes during program execution, the memory management unit changes the mapping function and transfers the data between disk and memory.
- Thus, during every memory cycle, an address processing mechanism determines whether theaddressed in function is in the physical memory unit.
- If it is, then the proper word is accessed and execution proceeds.

ROM:

- Both SRAM and DRAM chips are volatile, which means that they lose the stored information ifpower is turned off.
- Many application requires Non-volatile memory (which retain the stored information if power isturned off).
- **Example:** Operating System software has to be loaded from disk to memory which requires theprogram that boots the Operating System ie. It requires non-volatile memory.
- Non-volatile memory is used in embedded system.

(Or)

18. Illustrate the various performance considerations in memory system.

- Reduce the probability that two different memory blocks will contend for the same cache location.
- Additional cache levels,

Memory stall clock cycles = Read stall cycles + Write stall cycles

Read stall cycles = (Reads/ Program) x Read miss rate x Read miss penalty

Write stall cycles = (Writes/ Program x Write miss rate x Read miss penalty) + Write buffer stalls

Simplifying ignoring write buffer stalls which are not remarkable in case of enough large write buffers.

Memory stall clock cycle = Memory access/ program x miss rate x miss penalty Memory stall clock cycle = (Instructions/ program) x (misses/instruction) x miss penalty.

Dynamic Memory System

- The physical implementation is done in the form of Memory Modules.
- If a large memory is built by placing DRAM chips directly on the main system printed circuit board that contains the processor, often referred to as Motherboard; it will occupy large amount of space on the board.
- These packaging consideration have led to the development of larger memory units known as SIMM's and DIMM's.
    * SIMM-Single Inline memory Module
    * DIMM-Dual Inline memory Module
- SIMM and DIMM consists of several memory chips on a separate small board that plugs verticallyinto single socket on the motherboard.

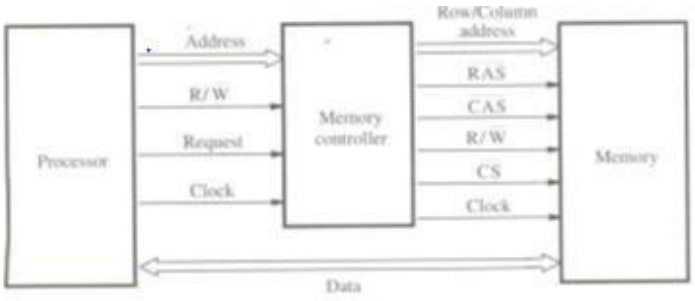
Memory System Consideration

- To reduce the number of pins, the dynamic memory chips use multiplexed address inputs.
- The address is divided into two parts. They are,
    * **High Order Address Bit** (Select a row in cell array and it is provided first and latched intomemory chips under the control of RAS signal).
    * **Low Order Address Bit** (Selects a column and they are provided on same address pins andlatched using CAS signals).
    * The Multiplexing of address bit is usually done by Memory Controller Circuit.
- The Controller accepts a complete address and R/W signal from the processor, under the control

of aRequest signal which indicates that a memory access operation is needed.

- The Controller then forwards the row and column portions of the address to the memory and generates RAS and CAS signals.
- It also sends R/W and CS signals to the memory.
- The CS signal is usually active low, hence it is shown as CS.

*

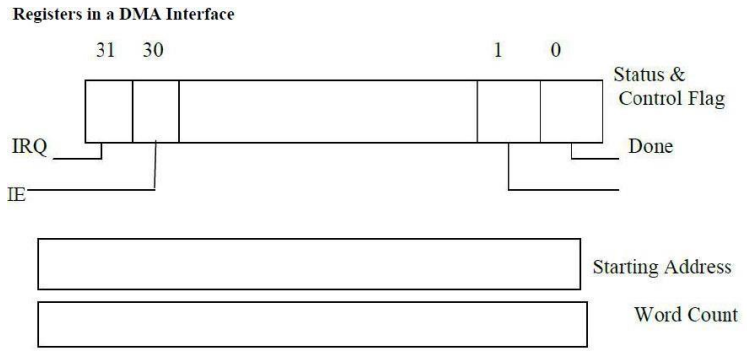


Memory Controller

UNIT-V

19. Draw and explain the function of DMA with suitable diagram.

- A special control unit may be provided to allow the transfer of large block of data at high speed directly between the external device and main memory, without continuous intervention by the processor. This approach is called DMA.
- DMA transfers are performed by a control circuit called the DMA Controller.
- To initiate the transfer of a block of words, the processor sends,
  * Starting address
  * Number of words in the block
  * Direction of transfer.



Cycle Stealing

- Requests by DMA devices for using the bus are having higher priority than processor requests.
- Top priority is given to high speed peripherals such as Disk
- High speed Network Interface and Graphics display device.

Burst Mode

- The DMA controller may be given exclusive access to the main memory to transfer a block of datawithout interruption.
- This is known as Burst/Block ModeBus Master
- The device that is allowed to initiate data transfers on the bus at any given time is called the busmaster.

Bus Arbitration

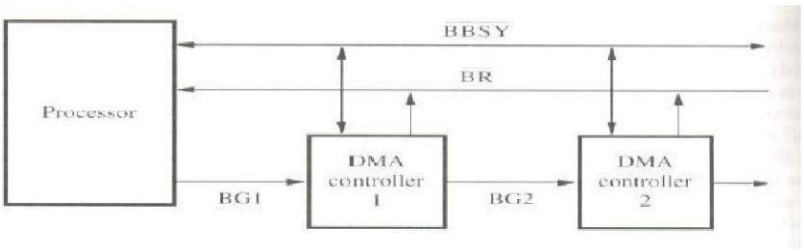
- It is the process by which the next device to become the bus master is selected and the bus mastership is transferred to it.

Types

- There are 2 approaches to bus arbitration. They are,
    * Centralized arbitration (A single bus arbiter performs arbitration)
    * Distributed arbitration (all devices participate in the selection of next bus master).

Centralized Arbitration

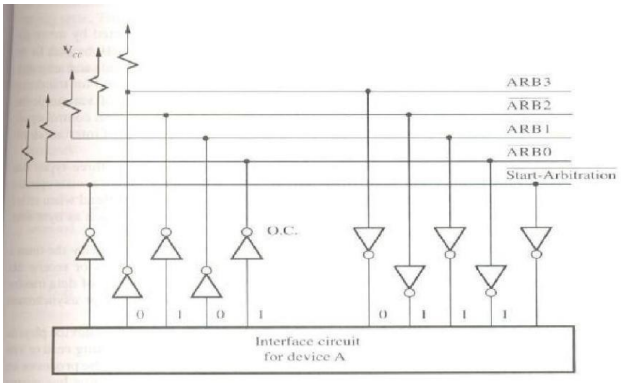
- Here the processor is the bus master and it may grants bus mastership to one of its DMA controller.
- A DMA controller indicates that it needs to become the bus master by activating the Bus Requestline (BR) which is an open drain line.



Sequence of signals during transfer of bus mastership for the devices

Distributed Arbitration

- It means that all devices waiting to use the bus have equal responsibility in carrying out thearbitration process.
- Each device on the bus is assigned a 4 bit id.

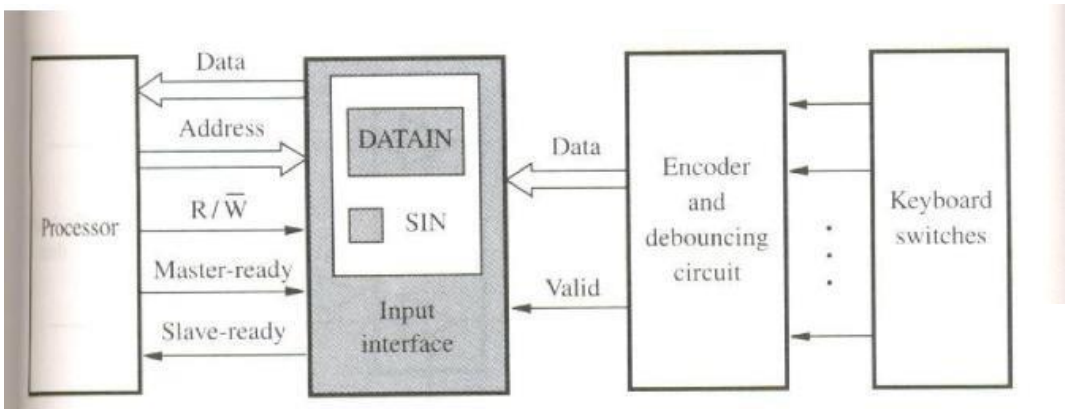


(Or)

20. Differentiate serial port with parallel port.

Parallel port

- A parallel port transfers data in the form of a number of bits, typically 8 or 16, simultaneously to orfrom the device.
- The connection between the device and the computer uses a multiple-pin connector and a cable withas many wires, typically arranged in a flat configuration.



- The output of the encoder consists of the bits that represent the encoded character and one signalcalled valid, which indicates the key is pressed.
- The information is sent to the interface circuits, which contains a data register, DATAIN and a statusflag SIN.
- When a key is pressed, the valid signal changes from 0 to1, causing the ASCII code to be loaded intoDATAIN and SIN set to 1.
- The status flag SIN set to 0 when the processor reads the contents of the DATAIN register.
- The interface circuit is connected to the asynchronous bus on which transfers are controlled usingthe Handshake signals Master ready and Slave-ready.

Serial port

- A serial port transmits and receives data one bit at a time.
- The serial format is much more convenient and cost-effective where longer cables are needed.
- A serial port is used to connect the processor to I/O devices that require transmission of data one bitat a time.

- The key feature of an interface circuit for a serial port is that it is capable of communicating in a bit-serial fashion on the device side and in a parallel fashion on the bus side.